CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

forming an isolation trench and a contact trench in a substrate, wherein a width of said isolation trench is less than a width of said contact trench;

depositing an insulating material over said isolation trench and said contact trench to substantially fill said isolation trench and reduce an effective width of said contact trench;

removing at least partially said insulating material from a bottom of said contact trench; and

filling in a conductive material into said contact trench to form a contact.

2. The method of claim 1, further comprising forming a buried conductive region in said substrate below said contact trench such that said buried region at least partially overlaps with said contact trench, said buried conductive region being conductively coupled to said contact.

3. The method of claim 2, wherein said buried conductive region is formed prior to the formation of said isolation trench and said contact trench.

4. The method of claim 3, wherein said contact trench is positioned so that said effective width at least partially overlaps with said buried conductive region.

5. The method of claim 3, wherein said contact trench is positioned so that said contact trench extends into said buried conductive region.

6. The method of claim 1, wherein at least one of said width of said contact trench and at least one deposition parameter during the deposition of the dielectric material is adjusted to obtain said effective width substantially in accordance with a predefined design value thereof.

7. The method of claim 1, wherein removing at least partially said insulating material includes anisotropically etching said insulating material.

8. The method of claim 7, wherein depositing said insulating material includes depositing an etch stop layer and depositing on said etch stop layer a dielectric layer.

9. The method of claim 1, wherein filling a conductive material in said contact trench includes depositing said conductive material over said contact trench and isolation trench and removing excess material of said conductive material by chemical mechanical polishing.

10. The method of claim 1, wherein said conductive material comprises a refractory metal.

11. The method of claim 1, wherein said conductive material comprises doped polysilicon.

12. The method of claim 9, wherein depositing said conductive material includes depositing a barrier layer on inner sidewalls of said contact trench.

13. The method of claim 3, further comprising implanting a dopant species into said buried region prior to at least partially removing said dielectric material from the bottom of said contact trench.

14. The method of claim 3, further comprising implanting a dopant species into said buried region after at least partially removing said dielectric material from the bottom of said contact trench.

15. The method of claim 2, wherein said buried region is formed after forming said isolation trench and said contact trench.

16. The method of claim 15, wherein ions are implanted into said substrate below said contact trench through said insulating layer to form said buried region.

17. The method of claim 15, wherein ions are implanted into said substrate below said contact trench after at least partially removing said insulating layer at the bottom of said contact trench to form said buried region.

18. A semiconductor device, comprising:

a substrate;

a first trench formed in said substrate and extending to a first depth, said first trench having a first width;

a second trench formed in said substrate and extending to said first depth, said second trench having a second width that is less than said first width;

insulating sidewall spacers formed on sidewalls of said first trench;

a conductive material filled in said first trench; and

an insulating material filled in said second trench.

19. The semiconductor device of claim 18, further comprising a buried conductive region formed in said substrate adjacent to said first trench.

20. The semiconductor device of claim 18, wherein said second trench is configured as an isolation structure to separate neighboring circuit elements of an integrated circuit.

21. The semiconductor device of claim 18, wherein said sidewall spacers comprise at least one of silicon dioxide and silicon nitride.

22. The semiconductor device of claim 18, wherein said conductive material comprises a refractory metal.

23. The semiconductor device of claim 22, further comprising a barrier layer formed on said sidewall spacers and a bottom of said first trench.

24. The semiconductor device of claim 18, wherein said conductive material comprises doped polysilicon.